UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,123	12/09/2003	Tatsuo Sengoku	009683-488	4345

21839 7590 07/12/2005

BUCHANAN INGERSOLL PC
(INCLUDING BURNS, DOANE, SWECKER & MATHIS)
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
PRUCHNIC, STANLEY J	
ART UNIT	**PAPER NUMBER**
2859	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/730,123	SENGOKU ET AL.
	Examiner	Art Unit
	Stanley J. Pruchnic, Jr.	2859

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *4-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Applicant's election without traverse of Group I (Claims 1-3) in the reply filed on 13 December 2004 is acknowledged.

3. Claims 4-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 13 December 2004.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Response to Arguments

5. Applicant's arguments, see the Remarks, filed 28 April 2005, with respect to the rejection(s)of claim(s) 1-3 under 35 U.S.C. § 103(a) have been fully considered and are persuasive.

Applicant's argument that Ebihara *et al.* (U. S. Patent No. 4,237,420, **EBIHARA**) does not disclose a pulse width measurement circuit receiving a signal from a logic circuit as claimed by Applicant in Claim 1 is persuasive in view of the fact that the Examiner mis-labeled counter 34 as a Schmitt trigger circuit in the Office Action mailed 02 February 2005.

Moreover, Applicant is correct in stating that the output of inverter 18 is output to pulse addition circuit 33 (Fig. 2), and that the pulse width measurement circuit 44 of

EBIHARA does not include a Schmitt trigger as claimed by Applicant in Claim 1. Instead, EBIHARA uses a counter 26 and other logic circuit elements for measurement of a pulse width.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of previously cited prior art.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebihara *et al.* (U. S. Patent No. 4,237,420, hereinafter **EBIHARA**) in view of **MEHNERT** (U. S. Patent No. 4,873,518 A) and JP7/326714 (hereinafter **NISHIGAKI**).

Regarding Claim 1, **EBIHARA** discloses a temperature detection circuit (Fig. 1) including:

> a signal output circuit **(22)** outputting a first signal **(a)** having at least one rising or falling portion;

a delay circuit **(18)** formed of at least one inverter **(18)** to output a delayed version **(f)** of said first signal;

a logic circuit **(12)** receiving said first signal and said delayed version of said first signal;

a pulse width measurement circuit **(23)** outputting

a *signal asserted* **(Rx)** in response to

a *signal received* **(b)** from said logic circuit

having a pulse with a width of no less than a predetermined width corresponding to a temperature desired to be detected; and

a latch circuit **(counter 26)** latching a signal output from said pulse width measurement circuit.

EBIHARA further discloses an integration circuit **(capacitor 16; resistor 14)** receiving a signal output from said logic circuit **(NOR gate 12)**. The circuit including inverter **(18)** functions as described by EBIHARA in Col. 2, Lines 28-66: One or both of Resistor 14 and Capacitor 16 varies linearly with temperature (Col. 2, Lines 47-56). The input threshold of inverter 18, in combination with the integration circuit temperature dependence, results in the output pulse "b" having a width related to temperature, as described by EBIHARA.

EBIHARA further discloses a pulse width measurement circuit 23 including a source of clock pulses Cx combined with the output pulse "b" at the AND gate so that counter 26 will count clock pulses while the AND gate is enabled by the pulse "b", thus measuring the width of the temperature-dependent pulse width.

EBIHARA as described above, does not disclose said pulse width measurement circuit **(23) having**

an integration circuit receiving a signal output from said logic circuit and

a Schmitt trigger circuit receiving a signal output from said integration circuit, said Schmitt trigger circuit having a trigger potential set to have a value corresponding to said predetermined width,

as claimed by applicant in Claim 1.

MEHNERT discloses embodiments of a pulse width measurement (discrimination) circuit 20 (Fig. 1) that is evidence of the art recognized equivalence (Col. 9, Lines 58-65) of a purely digital form (Fig. 2) including a counter and (as shown in Fig. 3) an analog/digital form including an "RC-member 60" (Col. 9, Lines 58-68), which is an integrating circuit as claimed by Applicant in Claim 1, and MEHNERT further discloses a Schmitt trigger circuit **(70)** receiving a signal output from said integration circuit 60, said Schmitt trigger circuit having a trigger potential set to have a value corresponding to said predetermined width (Col. 10, Lines 27-35), the width being set by the selected values of resistor 66 and capacitor 67 (*e.g.,* for "RC-member 60", the width being 90 microseconds).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a pulse width measurement circuit, as taught by **MEHNERT,** including an integration circuit receiving the signal "b" output from said logic circuit 18 and a Schmitt trigger circuit receiving a signal output from said integration circuit, said Schmitt trigger circuit having a trigger potential set to have a value corresponding to said predetermined width (predetermined by the integration circuit) for the pulse width measurement circuit of **EBIHARA,** including the counter, in order to perform the same function as the width pulse measurement circuit 23 of EBHARA, since they are art recognized equivalents used for measuring pulse width as taught by **MEHNERT** and the use of the RC integrator circuit would allow the output to be adjusted for a desired temperature.

EBIHARA as described above, does not explicitly disclose said circuit is a semiconductor integrated circuit as claimed by applicant in Claim 1. **EBIHARA** as described above, does not claim the components located on semiconductor integrated circuits as claimed by Applicant in claims 2-3.

NISHIGAKI discloses components on separate semiconductor integrated circuits, *e.g.,* the buffer circuit (inverter) 50 is located on a CPU in order to detect that

chip's internal temperature. Moreover, it is well known in the art of temperature sensing that the pulse width measurement circuit would be affected by temperature changes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to shift the positions of these components, in order to keep the pulse width measurement circuit away from the hottest areas so it will have more accurate results, and based on the intended use for the temperature dependent oscillator to measure the temperature of the CPU chip as taught by **NISHIGAKI**.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in a form PTO-892 and not mentioned above disclose related temperature sensing devices and methods of signal detection:

- LEMMENS (U. S. Patent No. 5,708,375 A); and
- YIN (U. S. Patent No. 6,695,475 B2).

Of the newly cited prior art:

- MEEHAN *et al.* (U. S. Patent No. 6,169,442 B1) discloses a related IC temperature monitoring chip including setting status registers (latch); and
- DARMAWASKITA *et al.* (U. S. Patent No. 5,899,570 A) discloses a temperature sensor including a temperature dependent oscillator which uses a Schmitt trigger 30 in combination with an integrated circuit 34.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanley J. Pruchnic, Jr., whose telephone number is **(571) 272-2248**. The examiner can normally be reached on weekdays (Monday through Friday), the best hours being from 8:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez (Art Unit 2859) can be reached at **(571) 272-2245**. The Central FAX Number for *all official communications*, as of July 15, 2005, is **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application or proceeding may be directed to the official USPTO website at **www.uspto.gov** or you may call the **USPTO Call Center** at **800-786-9199** or 703-308-4357. The Technology Center 2800 Customer Service FAX phone number is (703) 872-9317.

The cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site, from the Office of Public Records and from commercial sources.

Private PAIR provides external customers Internet-based access to patent application status and history information as well as the ability to view the scanned images of each customer's own application file folder(s).

For inquiries relating to Patent e-business products and service applications, you may call the ***Patent Electronic Business Center (EBC)*** at **703-305-3028 or toll free at 866-217-9197** between the hours of **6 a.m. and midnight Monday through Friday EST,** or by e-mail at: **ebc@uspto.gov.** Additional information is available on the Patent EBC Web site at: **http://www.uspto.gov/ebc/index.html.**

Stanley J. Pruchnic, Jr.
7/10/05

GAIL VERBITSKY
PRIMARY EXAMINER